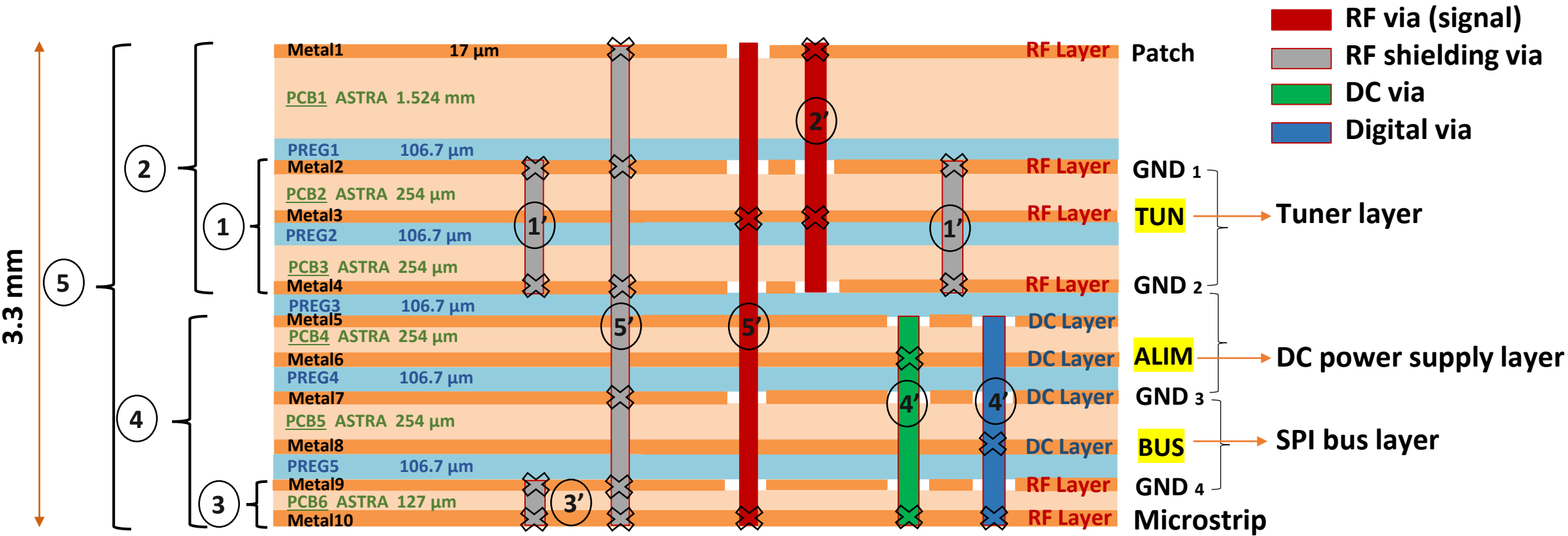


# PCB Stack-Up



## Manufacturing plan:

1, 2, 3, 4, 5: Stacking  
1', 2', 3', 4', 5': Drilling

PCB dimensions	Center frequency	Substrate	Permittivity $\epsilon_r$	Dielectric loss tangent	Coefficient of Thermal Expansion (CTE in ppm/°C)	Permittivity Preg
340 X 400 mm <sup>2</sup>	8.2 GHz	AstraMT77	3	0.0017	12 (X) , 12 (Y), 50 - 70 (Z)	2.95

## Manufacturing plan description (proposal)

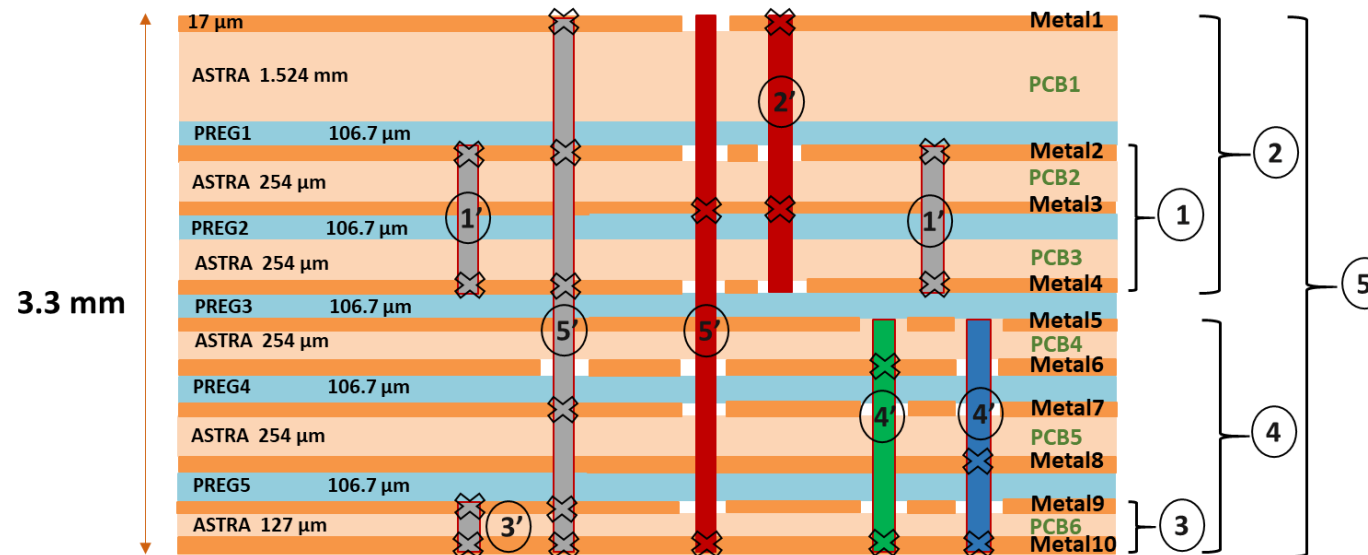
**Sequence 1:** Fabrication of Metal2 and Metal4 on PCB2 (double-sided) and Metal4 on PCB3 (single-sided). Stacking of PCB2 and PCB3, followed by via drilling between layers 2 and 4.

**Sequence 2:** Fabrication of Metal1 on PCB1, followed by its stacking with Sequence 1. Then, via drilling between layers 1 and 4.

**Sequence 3:** Fabrication of Metal9 and Metal10 on PCB6. Then via drilling between layers 9 and 10.

**Sequence 4:** Fabrication of Metal5 and Metal6 on PCB4. Fabrication of Metal7 and Metal8 on PCB5. Stacking of PCB4 and PCB5, followed by its stacking with sequence 3. Then via drilling between layers 5 and 10.

**Sequence 5:** Stacking of sequence 2 and 4. Then via drilling between layers 1 and 10.



- 9 different circuit schematic repeated on the whole panel (3 RF via diameter, with 3 clearances around the via)

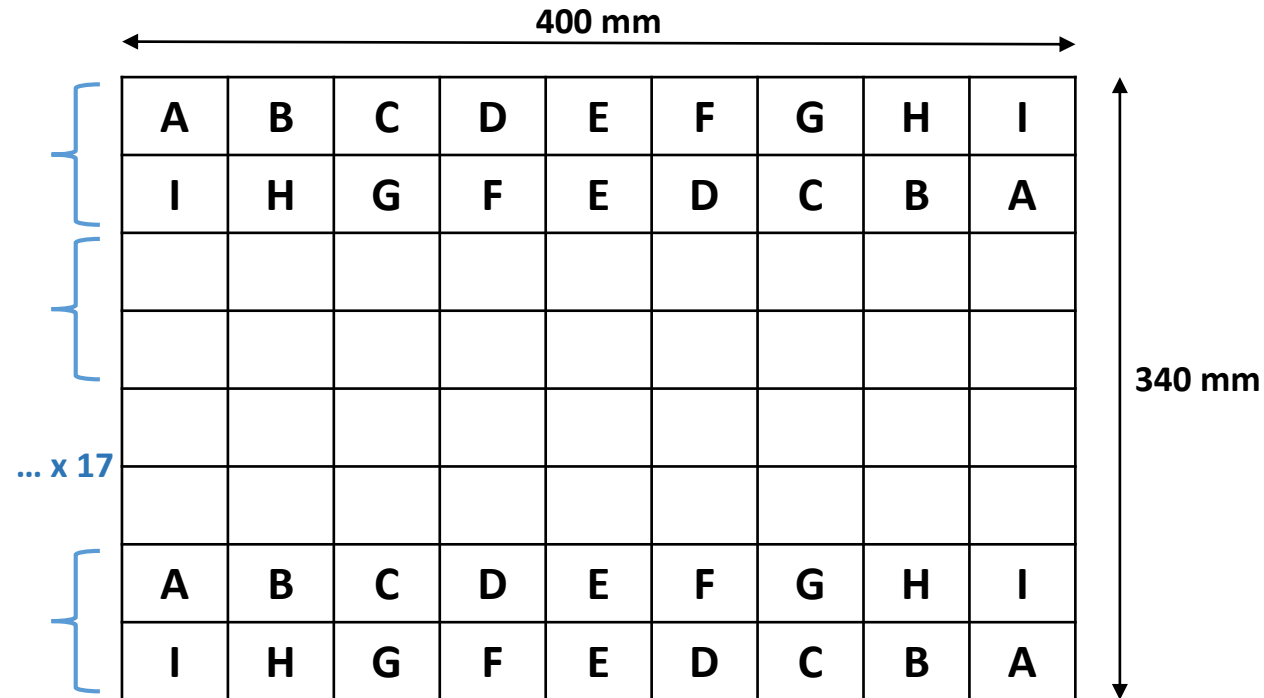
Diameter Via RF (mm)	Clearance(mm)
D1 = 0,7	gap1 = 0,3
	gap2 = 0,4
	gap3 = 0,5
D2 = 0,6	gap1 = 0,3
	gap2 = 0,4
	gap3 = 0,5
D3 = 0,5	gap1 = 0,3
	gap2 = 0,4
	gap3 = 0,5

Numerical parameters

Via	Length (mm)	Diameter (mm)	Minimum Clearance (mm)
1'	0,6487	0,3	0,21
2'	2,3	0,4	0,3
3'	0,161	0,3	1
4'	0,9334	0,6	0,3
5'	3,3	$\Phi 1 = 0,5$ $\Phi 2 = 0,6$ $\Phi 3 = 0,7$ $\Phi 4 = 1,4$ $\Phi 5 = 1,5$	0,3

Minimum clearance of coplanar waveguide	0,2 mm
---	--------

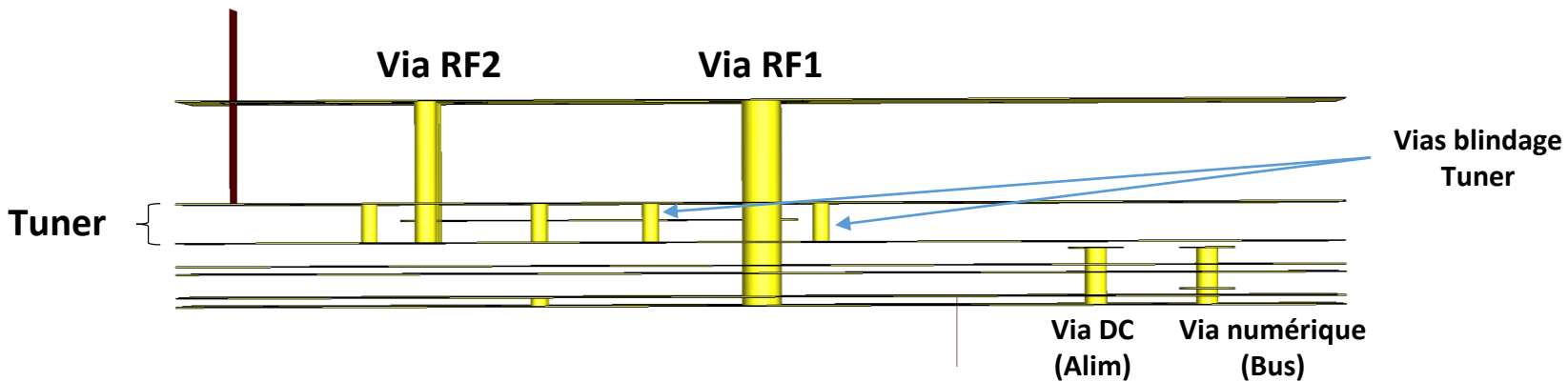
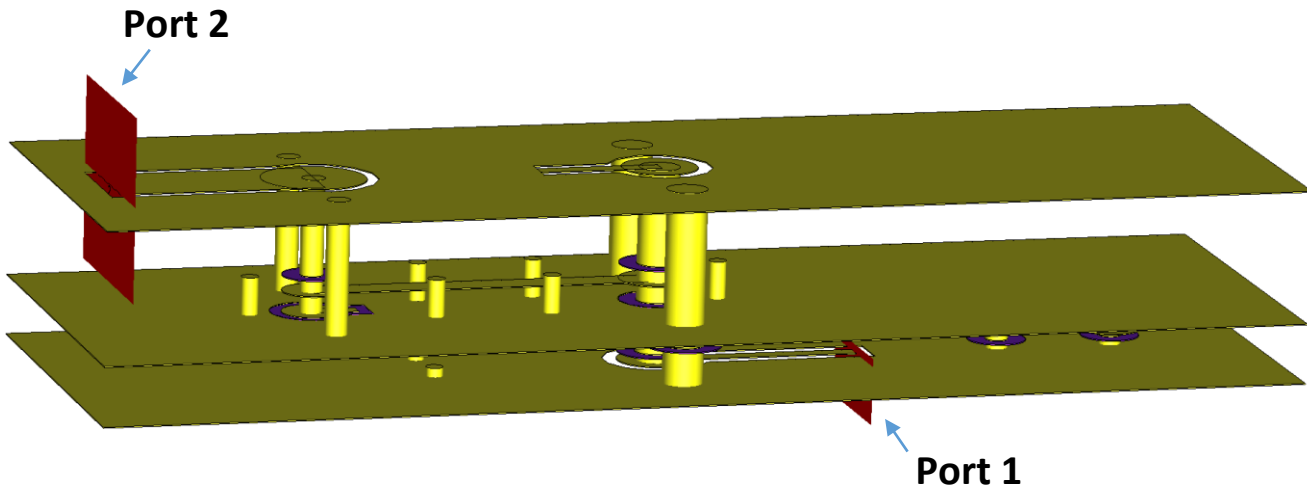
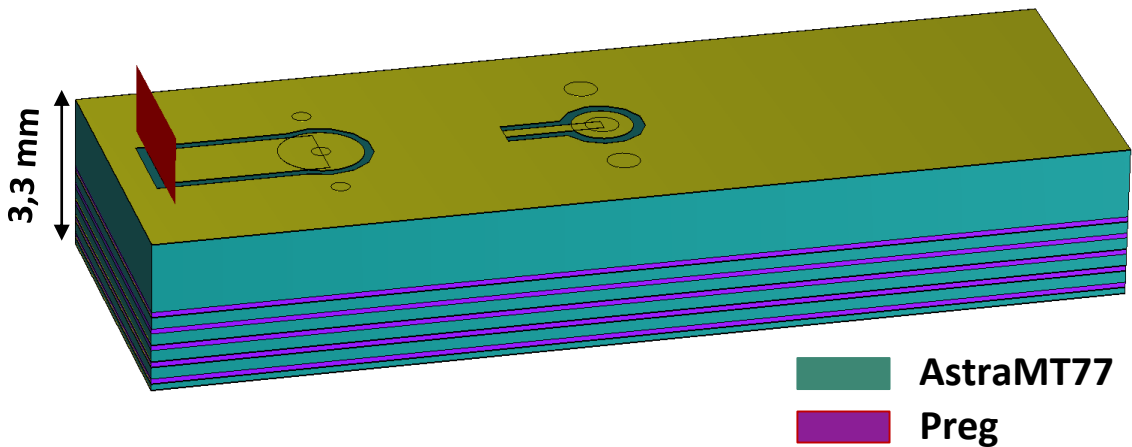
## ➤ Location of the different circuits on the panel:



➔ 306 elements

- A: D1 = 0,7 & gap1 = 0,3
- B: D1 = 0,7 & gap2 = 0,4
- C: D1 = 0,7 & gap3 = 0,5
- D: D2 = 0,6 & gap1 = 0,3
- E: D2 = 0,6 & gap2 = 0,4
- F: D2 = 0,6 & gap3 = 0,5
- G: D3 = 0,5 & gap1 = 0,3
- H: D3 = 0,5 & gap2 = 0,4
- I: D3 = 0,5 & gap3 = 0,5

# CAD view (only 1 sample circuit of the panel)



Diameter via RF2	0,4 mm
L_stripline	6 mm
gapViasRF2	0,3 mm
Rslot_viaRF2	0,2 mm
Rslot_viaRF1	0,25 mm
W_microstrip_sup	1,555 mm
W_microstrip_bottom	0,291 mm

# Panel (1 single PCB with all the circuits for tests)

## Panel view

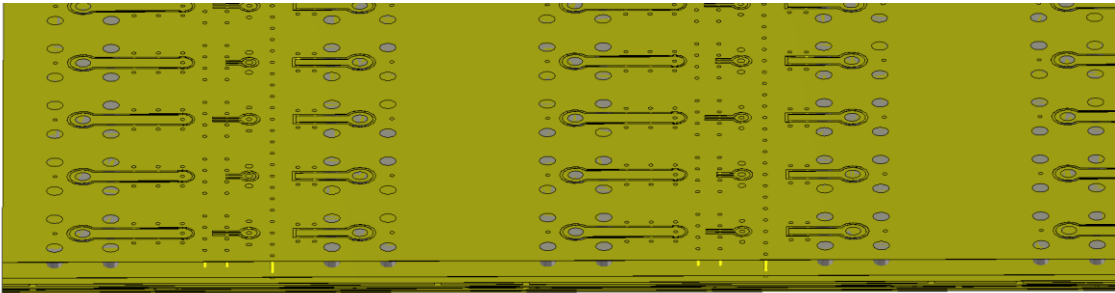
A	B	C	D	E	F	G	H	I
I	H	G	F	E	D	C	B	A
A	B	C	D	E	F	G	H	I
I	H	G	F	E	D	C	B	A

400 mm

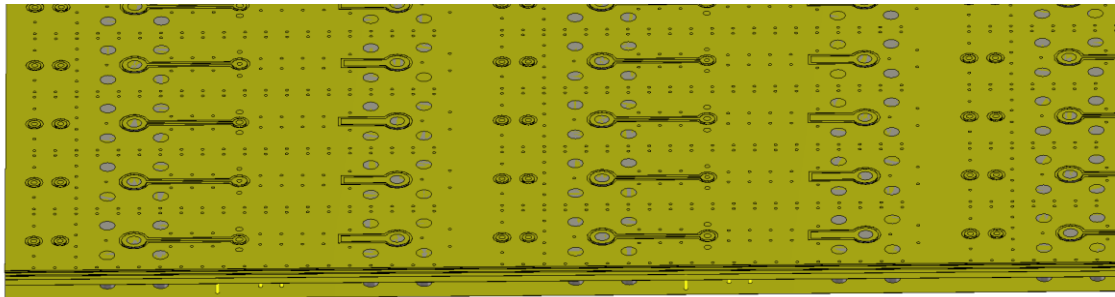
340 mm

➔ 306 elements

## Top view



## Bottom view



# Panel (1 single PCB with all the circuits for tests)



Co-funded by  
the European Union



## Gerber files (metallic layers)

